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10ES33

Third Semester B.E. Degree Examination, June/July 2014
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. $A_8A_4A_2A_1$ is an 8421 BCD input to a logic circuit whose output is a 1 when $A_8 = 0$, $A_4 = 0$ and $A_2 = 1$, or when $A_8 = 0$ and $A_4 = 1$. Design the simplest possible logic circuit. **(08 Marks)**

b. Simplify the given function using K-MAP
$\sum m(0, 2, 3, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 26, 27)$. **(06 Marks)**

c. Design a three-input, one-output minimal two-level gate combinational circuit which has an output equal to 1 when majority of its inputs are at logic 1 and has an output equal to 0 when majority of its inputs are at logic 0. **(06 Marks)**

2 a. Find a minimal sum for the following Boolean function using decimal Quine-Moclusky method and prime implicant table reduction $F = \sum(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$. **(10 Marks)**

b. For the given Boolean function, determine a minimal sum using MEV techniques using a, b, c as the map variables $f = \sum(3, 4, 5, 6, 7, 8, 9, 12, 13, 15)$. **(05 Marks)**

c. Find a minimal sum for the following Boolean function using MEV technique with a, b and c as the map variables $f(\alpha, \beta, a, b, c) = \alpha\overline{a}\overline{b}\overline{c} + \alpha\overline{a}\overline{b}c + \alpha a\overline{b}\overline{c} + \beta\overline{a}\overline{b}c + \beta a\overline{b}\overline{c} + a\overline{b}\overline{c} + a\overline{b}c$. **(05 Marks)**

3 a. Develop the logic diagram of a 2 to 4 decoder with the following specifications:
i) Active low enable input; ii) Active high encoded outputs. Draw the IEEE symbol. **(06 Marks)**

b. Design a combinational circuit to convert BCD to excess – 3. **(08 Marks)**

c. Write the condensed truth table for 0, 4, to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs. **(06 Marks)**

4 a. How does the look-ahead carry adder speed up the addition process? **(10 Marks)**

b. Implement a 12-bit comparator using IC7485. **(04 Marks)**

c. Implement $u = ad + b\overline{c} + bd$, using and 4 – 1 MUX using ab as select inputs. **(06 Marks)**

PART – B

5 a. Explain the working of pulse-triggered JK flip-flop with typical JK flip-flop waveforms. **(08 Marks)**

b. Explain switch debouncer using S-R latch with waveforms associated with switch debouncer. **(08 Marks)**

c. How do you convert J-K flip-flop to S-R flip-flop? **(04 Marks)**

6 a. Explain the working of universal shift register with the help of logic diagram and mode control table. **(10 Marks)**

b. Design a synchronous counter to count from 0000 to 1001 using JK flip-flops. **(10 Marks)**

7 a. A sequential circuit has two flip-flop A and B, two inputs x and y, and an output Z. The flip-flop input function and the circuit output functions are as follows:
$J_A = xB + \overline{yB}$; $K_A = x\overline{yB}$; $J_B = x\overline{A}$; $K_A = x\overline{y} + A$; $Z = xyA + \overline{xy}B$. Obtain the logic diagram, state-table and state equations, also state diagram. **(10 Marks)**

b. Realize the system represented by the state diagram shown in Fig.Q.7(a). Using D-flip-flop. **(10 Marks)**

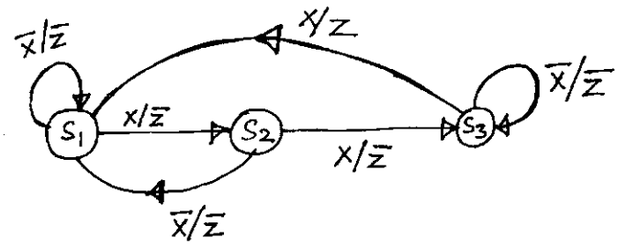

Fig.Q.7(a)

8 a. Design and implement a synchronous 3 bit up/down counter using J-K flip flops. **(10 Marks)**

b. What do you mean by the Moore model and Melay model of the state diagram? **(04 Marks)**

c. Draw the state diagram of a Mealy machine to detect as input sequence 10110 with overlap. An output 1 is to be generated when the sequence is detected. **(06 Marks)**

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